

NCE N-Channel Super Trench Power MOSFET

Description

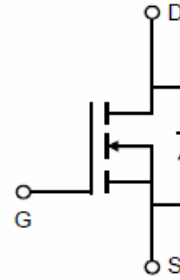
The NCEP4045GU uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = 40V, I_D = 45A$
 $R_{DS(ON)} = 6.0m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 8.5m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View

Bottom View

100% UIS TESTED!

100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP4045GU	NCEP4045GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	45	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	31.8	A
Pulsed Drain Current	I_{DM}	125	A
Maximum Power Dissipation	P_D	28	W
Derating factor		0.22	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	4.5	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	6	6.6	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	8.5	10	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$		30	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	831	-	PF
Output Capacitance	C_{oss}		-	318	-	PF
Reverse Transfer Capacitance	C_{rss}		-	24	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=20A$ $V_{GS}=10V, R_G=1.6\Omega$	-	6	-	nS
Turn-on Rise Time	t_r		-	2.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	17.6	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	20	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ ^(Note 3)	-	11	-	nS
Reverse Recovery Charge	Q_{rr}		-	19	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}C, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

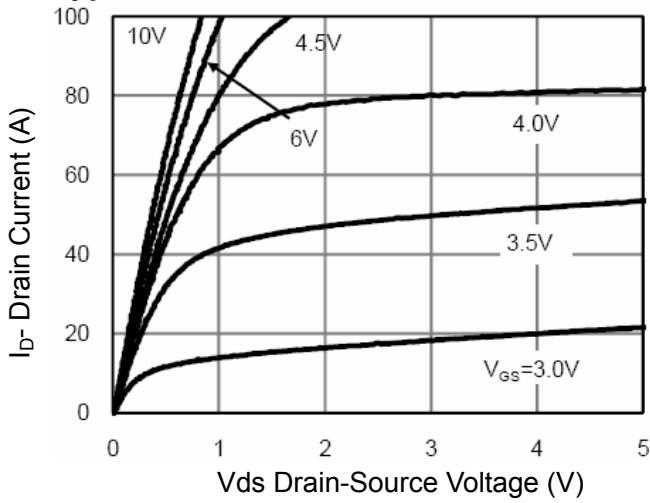


Figure 1 Output Characteristics

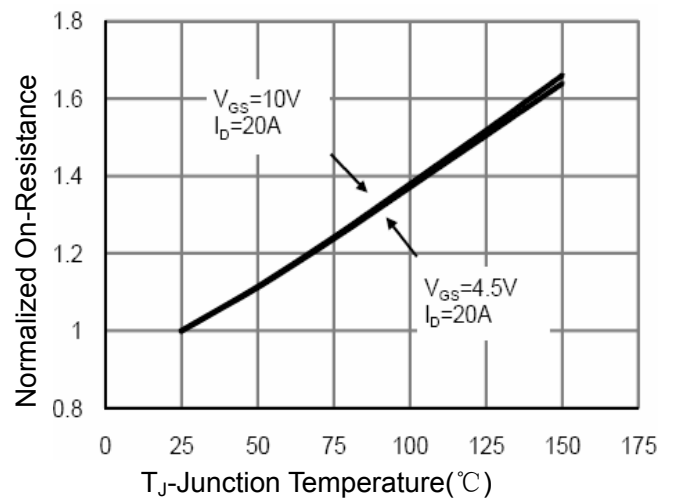


Figure 4 R_{dson} -Junction Temperature

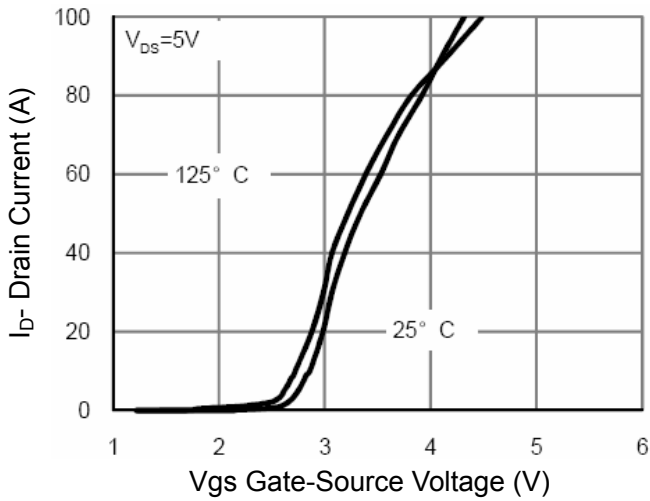


Figure 2 Transfer Characteristics

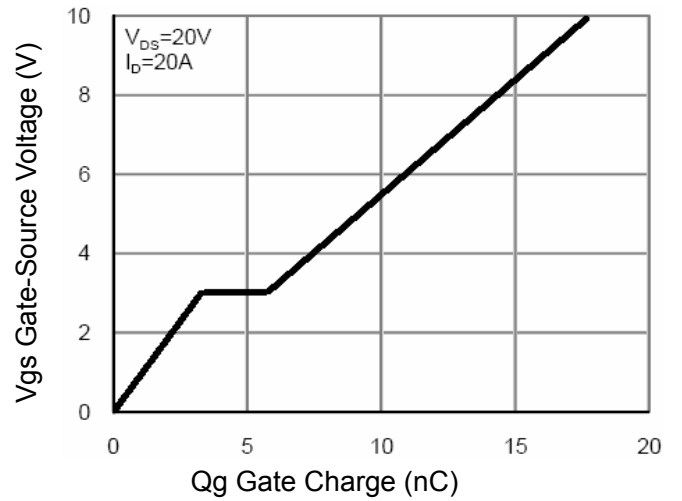


Figure 5 Gate Charge

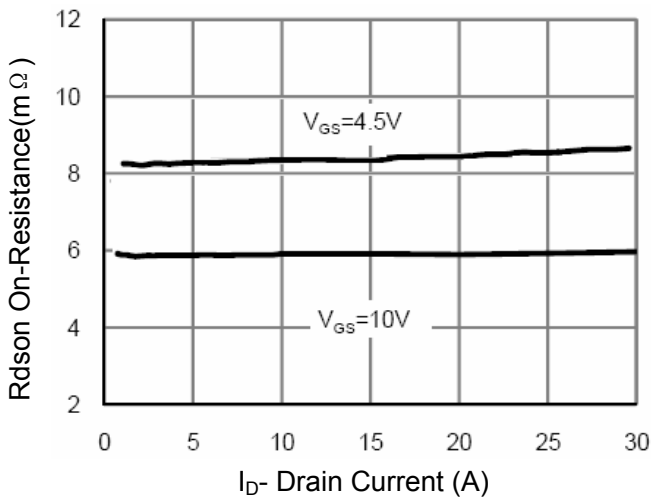


Figure 3 R_{dson} - Drain Current

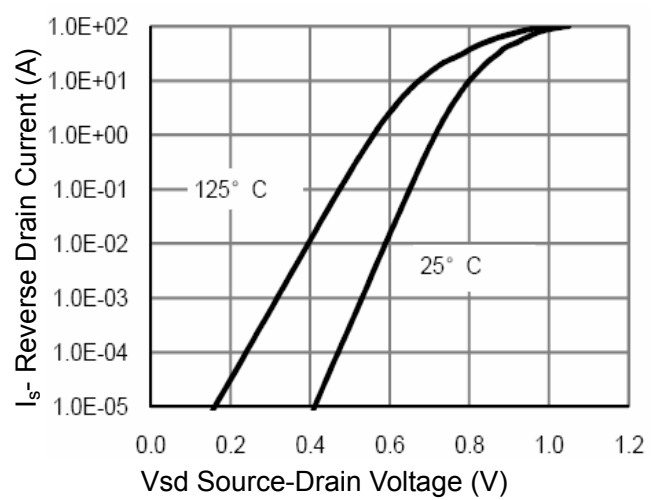


Figure 6 Source- Drain Diode Forward

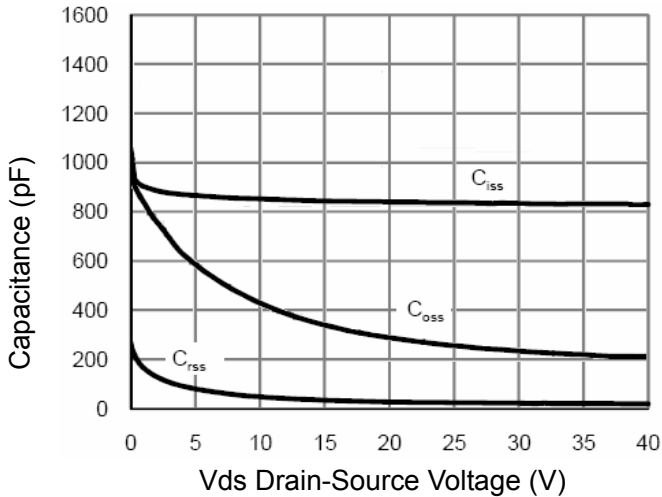


Figure 7 Capacitance vs Vds

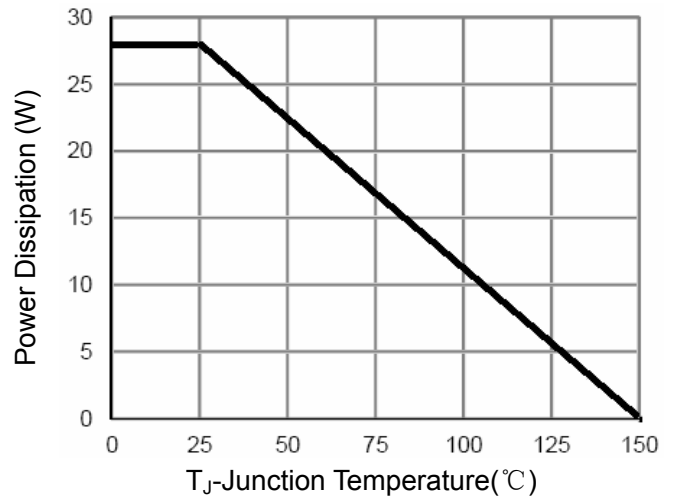


Figure 9 Power De-rating

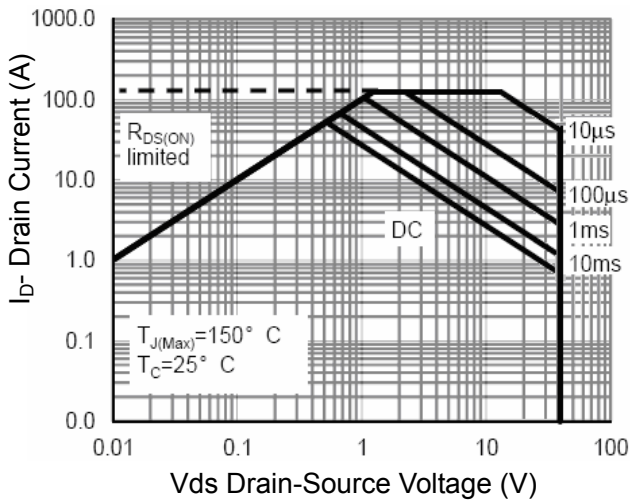


Figure 8 Safe Operation Area

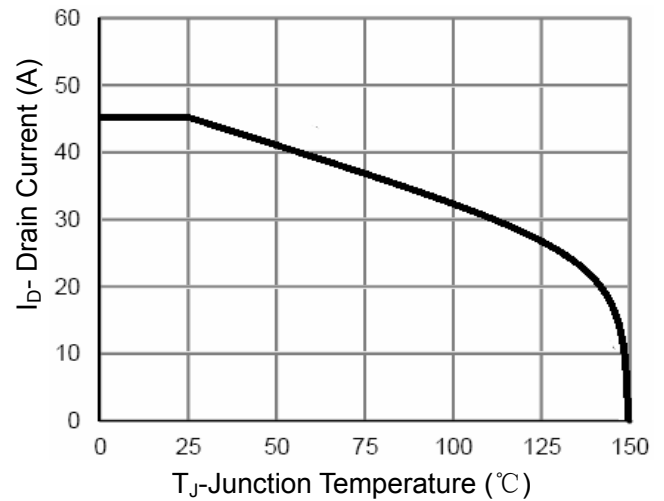


Figure 10 Current De-rating

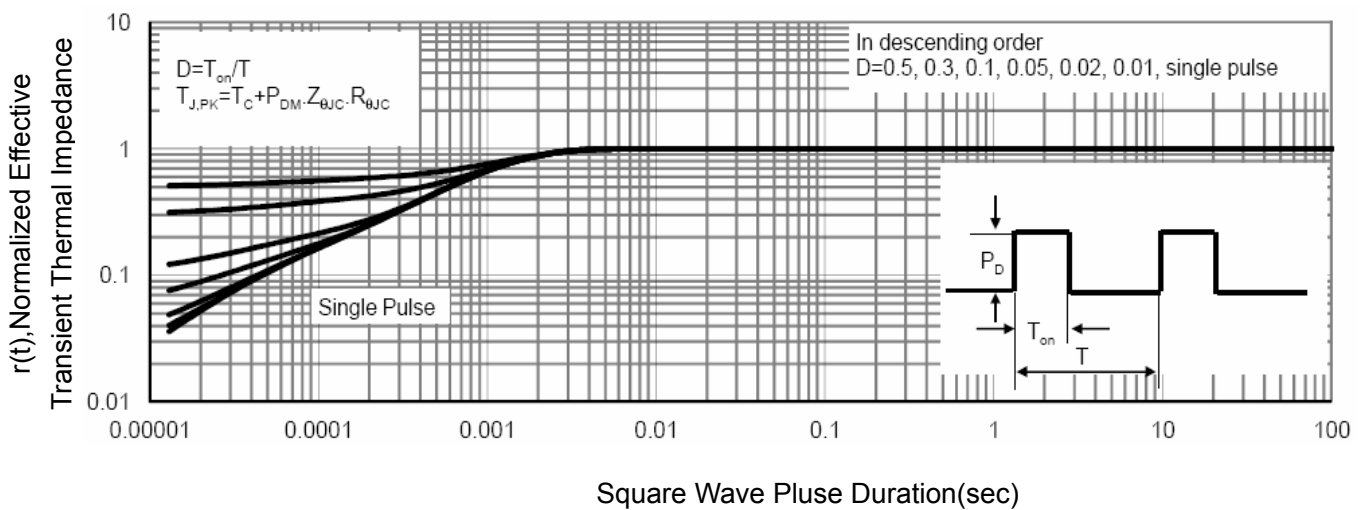
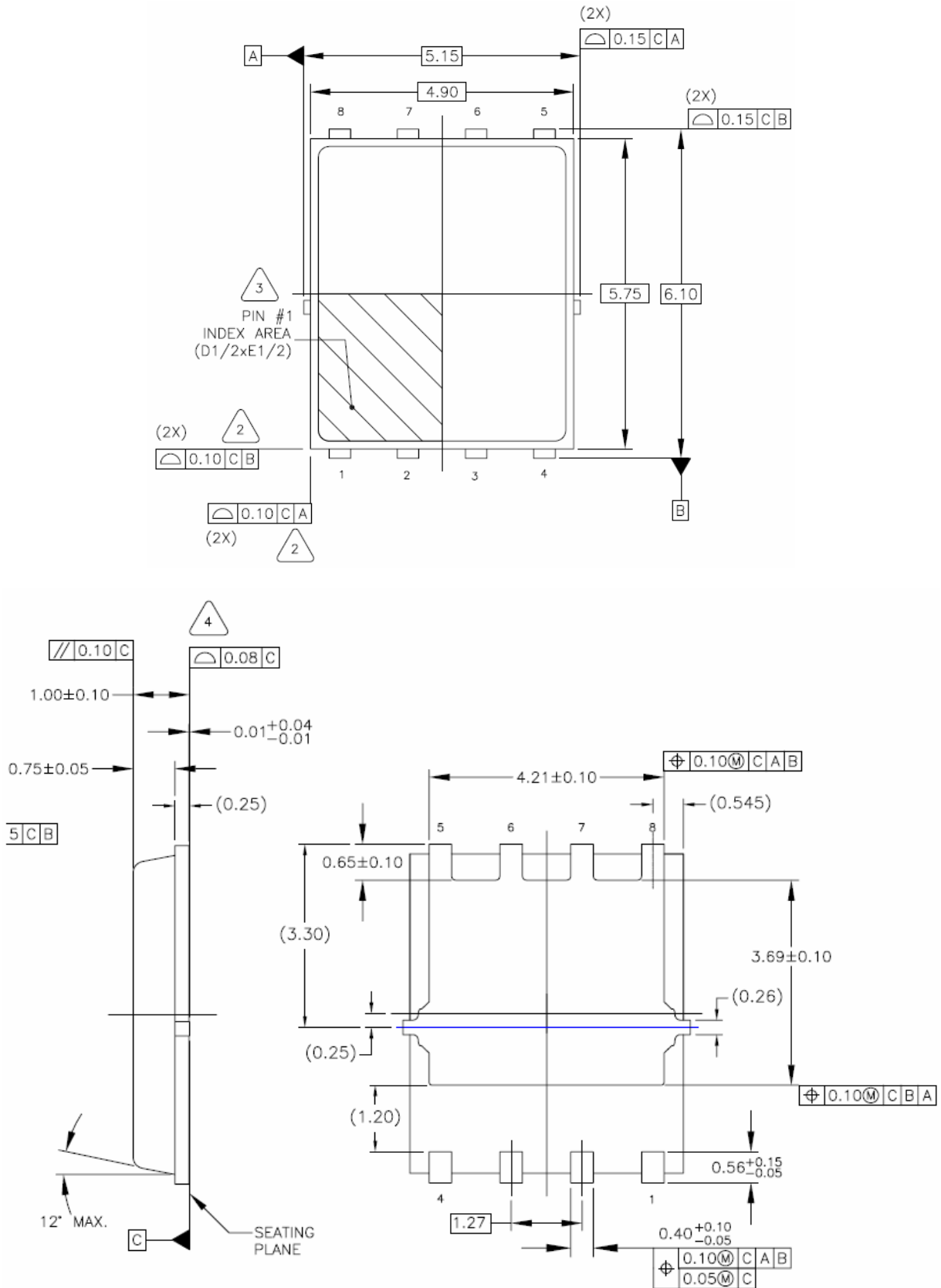


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



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